What is claimed is:

1. An integrated circuit to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the integrated circuit comprising:

a plurality of memory blocks, each of the memory blocks comprising a plurality of sub-memory blocks;

a plurality of data memory blocks corresponding to the memory blocks; and

a tag memory controlling unit, which writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address, wherein access to the same sub-memory block is not simultaneously performed when the write address and the read address are the same.

2. The integrated circuit of claim 1, wherein the sub-memory blocks are a set of memory cells for sharing a common word line or bit line.

3. The integrated circuit of claim 1, wherein in the sub-memory blocks, two or more word lines or bit lines cannot be simultaneously activated.

4. The integrated circuit of claim 1, wherein each of the data memory blocks has the same size as one sub-memory block.

5. The integrated circuit of claim 1, wherein if each of the data memory blocks has the same size as one sub-memory block, the data memory blocks have a number of columns and rows different from a number of columns and rows of the sub-memory block.

6. The integrated circuit of claim 1, wherein the tag memory controlling unit has a same number of decoding addresses as a number of addresses for decoding the data memory blocks.

7. The integrated circuit of claim 6, wherein the tag memory controlling unit has a number of columns and rows different from a number of columns and rows of the data memory blocks.

8. The integrated circuit of claim 1, wherein the tag memory controlling unit stores a data memory address indicating that data stored in the data memory blocks is originally data corresponding to one of the sub-memory blocks, and validity determination information for determining whether data stored in the data memory block is valid.

9. The integrated circuit of claim 8, wherein if the number of the sub-memory blocks is 2N, each address of the tag memory controlling unit includes N+1 data bits, and N-bit of the N+1 data bits indicates a data memory address, and

remaining 1-bit of the N+1 data bits indicates the validity determination information.

10. The integrated circuit of claim 1, wherein the data memory blocks have a direct mapping relation with the sub-memory blocks.

11. The integrated circuit of claim 1, wherein the data is input or output at a single data rate (SDR) or a double data rate (DDR).

12. A method for simultaneously performing a write operation and a read operation in an integrated circuit comprising a separate input and output, the method comprising:

determining if a write address and a read address have been input during a period of a clock signal;

determining if an upper address of the write address is the same as the upper address of the read address; and

performing a write operation and a read operation during the period of the clock signal.

13. The method of claim 12, further comprising:

determining if the write address and the read address are the same as a data memory address, when it is determined that the upper address of the write address and the upper address of the read address are the same.

14. The method of claim 13, wherein the write operation is performed in a data memory block and the read operation is performed in a sub-memory block when the one of the write address and the read address is not the same as the data memory address.

15. The method of claim 13, further comprising:

determining if one of the write address and the read address is coincident with the data memory address or if the write address and the read address are coincident with the data memory address.

16. The method of claim 15, wherein the read operation is performed in the data memory block and the write operation is performed in a sub-memory block when the write address and the read address are not coincident with the data memory address or when one of the read address and the write address are coincident with the data memory address the operation corresponding to the address coincident with the data memory address is performed in the data memory block and the operation corresponding to the address not coincident with the data memory address is performed in the sub-memory block.

17. The method of claim 12, further comprising:

determining if the write address and the read address are coincident with a data memory address, when it is determined that the upper address of the write address and the upper address of the read address are not the same.

18. The method of claim 17, wherein the write operation and the read operation are performed in different sub-memory blocks corresponding to the write address and the read address among selected memory blocks.

19. The method of claim 17, further comprising:

determining if one of the write address and the read address is coincident with the data memory address or if the write address and the read address are coincident with the data memory address.

20. The method of claim 19, wherein the read operation is performed in the data memory block and the write operation is performed in a sub-memory block when the write address and the read address are not coincident with the data memory address or when one of the read address and the write address are coincident with the data memory address the operation corresponding to the address coincident with the data memory address is performed in the data memory block and the operation corresponding to the address not coincident with the data memory address is performed in the sub-memory block.